

JEDEC STANDARD

0.6 V Low Voltage Swing Terminated Logic (LVSTL06)

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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0.6 V LOW VOLTAGE SWING TERMINATED LOGIC (LVSTL06)

(From JEDEC Board Ballot JCB-16-37, formulated under the cognizance of the JC-16 Committee on Interface Technology.

1 Scope

This standard defines power supply voltage range, dc interface, switching parameter and overshoot/undershoot for high speed low voltage swing terminated NMOS driver family digital circuits with 0.6V supply. The specifications in this standard represent a minimum set of interface specifications for low voltage terminated circuits.

The purpose of this standard is to provide a standard of specification for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users. Class 1 describes low V_{OH} (Nominal $V_{OH} = V_{DDQ} \cdot 0.5$) level terminated electrical characteristics. Class 2 describes high V_{OH} (Nominal $V_{OH} = V_{DDQ} \cdot 0.6$) level terminated electrical characteristics.

2 LVSTL system definition

LVSTL (Low Voltage Swing Terminated Logic) Driver and ODT System LVSTL I/O cell is comprised of pull-up, pull-down driver and a terminator. The basic cell is shown in **Figure 1**.

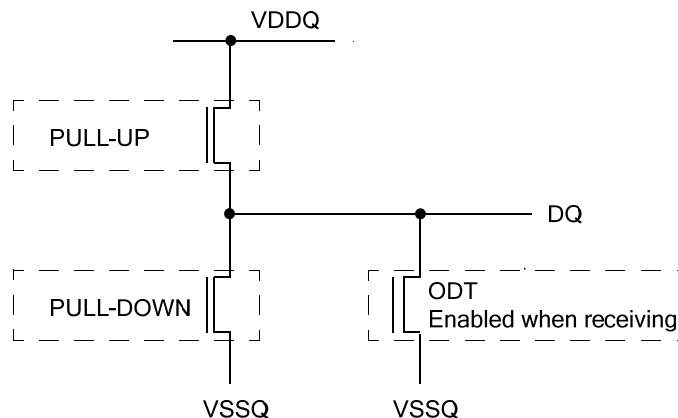


Figure 1 — LVSTL I/O Cell

2.1 Standard specifications

All voltages are referenced to ground except where noted.

2.2 Recommended DC Operating conditions

Table 1 — Recommended DC operating conditions

	Min	Nom	Max	Unit	
VDDQ	0.57	0.6	0.65	V	I/O Buffer Power

2.3 Pull Up Driver Characteristics for class 1 and class 2

Table 2 — Pull-Up Characteristics

VOH _{PU,nom}	VOH(mV)			VOH _{PU}			Unit
	Min	Nom	Max	Min	Nom	Max	
Class 1 VDDQ*0.5	270	300	330	0.9	1	1.1	VOH, nom
Class 2 VDDQ*0.6	325	360	395	0.9	1	1.1	VOH, nom

2.4 Data Input Characteristics for class 1 and class 2

Input levels are same for both class 1 and class 2

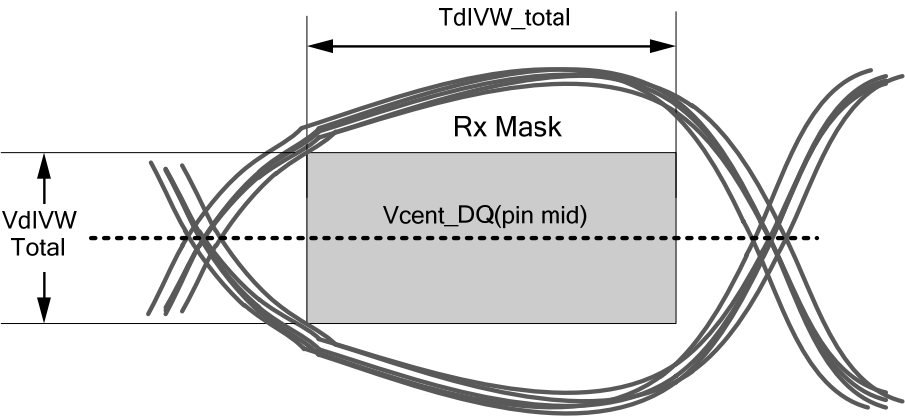
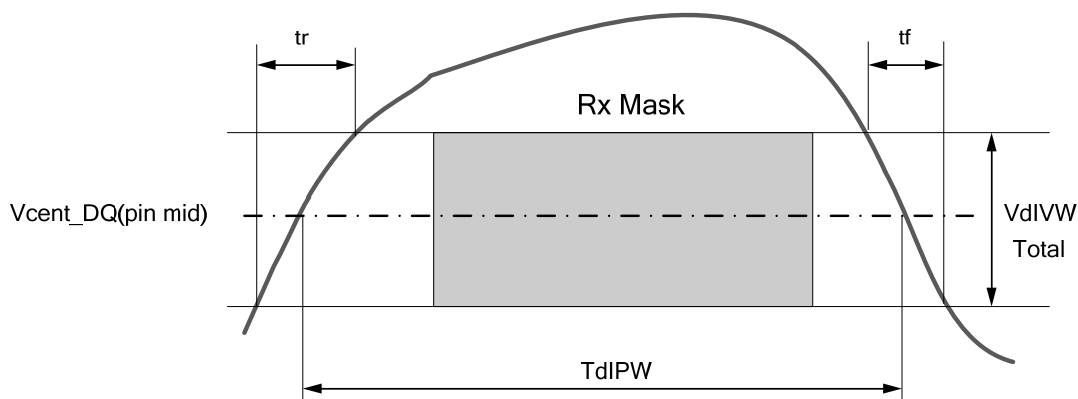


Figure 2 — DQ Receiver (Rx) mask

2.4 Data Input Characteristics for class 1 and class 2 (cont'd)



Note 1. $SRIN_dIVW = VdIVW_Total / (tr \text{ or } tf)$, signal must be monotonic within tr and tf range.

Figure 3 — DQ TdIPW definition (for each input pulse)

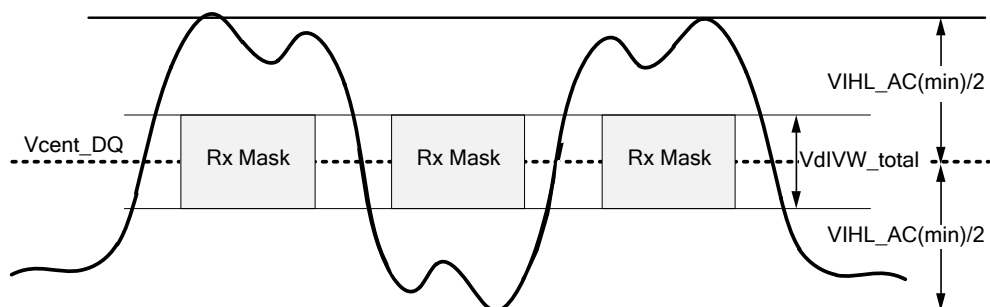


Figure 4 — DQ VIHL_AC definition (for each input pulse)

Table 3 — DQ Input Voltage

Symbol	Parameter	Range 1		Range 2		Unit
		Min	max	Min	max	
VdIVW_total	Rx Mask voltage - p-p total	-	140	-	120	mV
VIHL_AC	DQ AC input pulse amplitude pk-pk	180	-	170	-	mV

NOTE Each device specification defines Range 1 and Range 2 adaptation. Please refer to the device specification.

2.5 CA Input Characteristics for class 1 and class 2

Input levels are same for both class 1 and class 2.

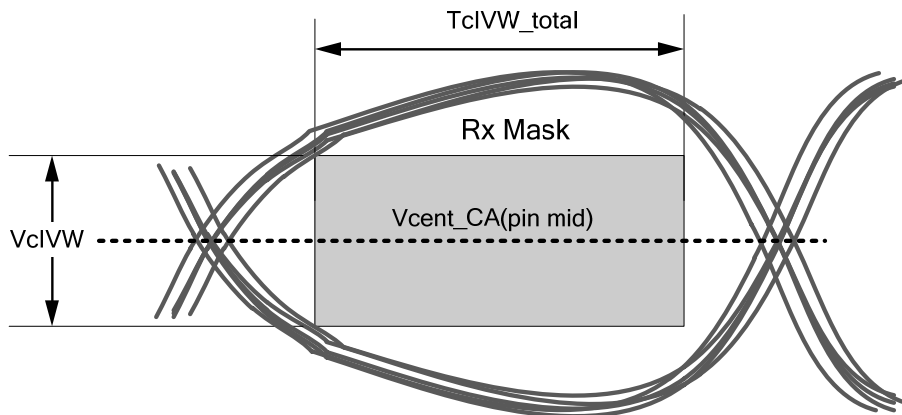


Figure 5 — CA Receiver(Rx) mask

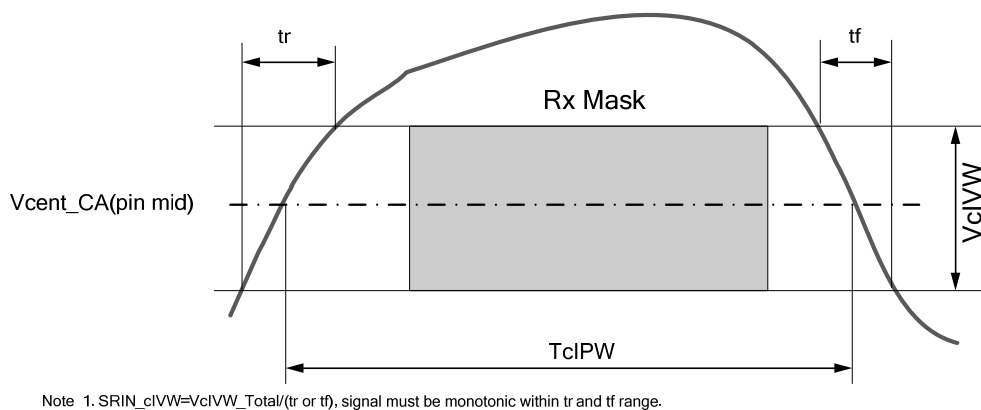


Figure 6 — CA TcIPW definition (for each input pulse)

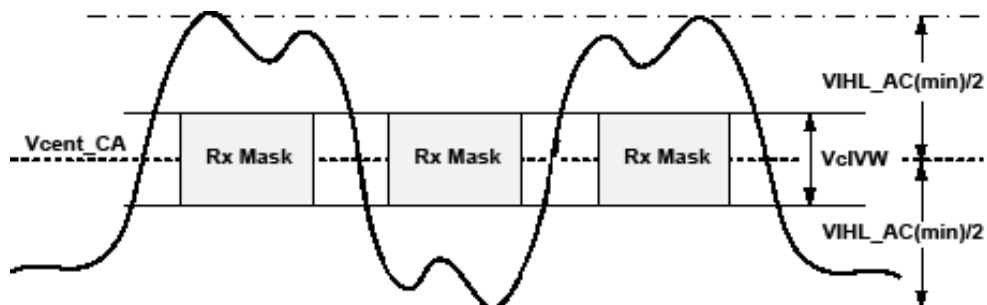


Figure 7 — CA VIH_L_AC definition (for each input pulse)

2.5 CA Input Characteristics for class 1 and class 2 (cont'd)

Table 4 — CMD/ADR, CS voltage definitions

Symbol	Parameter	Range 1		Range 2		Range 3		Unit
		min	max	min	max	min	max	
VcIVW	Rx Mask voltage - p-p	-	175	-	155	-	145	mV
VIHL_AC	CA AC input pulse amplitude pk-pk	210	-	190	-	180	-	mV

NOTE Each device specification defines Range 1, Range 2, and Range 3 adaptations. Please refer to the device specification.

2.6 DQS Differential Input Cross Point Voltage

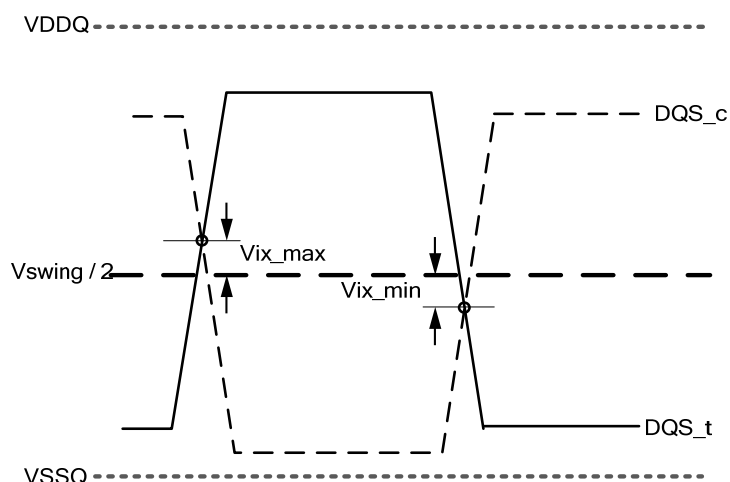


Figure 8 — DQS input Crosspoint voltage (Vix)

Table 5 — DQS input voltage crosspoint(Vix) ratio

Parameter	Symbol	Min	Max	Units	Notes
DQS Differential input crosspoint voltage ratio	Vix_DQS_ratio	-	20	%	1,2

NOTE 1 The Vix voltage is referenced to $V_{swing}/2(avg) = 0.5(V_{DQS_t} + V_{DQS_c})$ where the average is over **TBD**¹ UI.

NOTE 2 The ratio of the Vix pk voltage divided by V_{diff_DQS} : $Vix_DQS_Ratio = 100 * (Vix_DQS/V_{diff_DQS})$ where $V_{diff_DQS} \text{ pk-pk} = 2 * |V_{DQS_t} - V_{DQS_c}|$

¹ At time of publication the formulating committee has not defined the value.

2.7 Clock Differential Input Cross Point Voltage

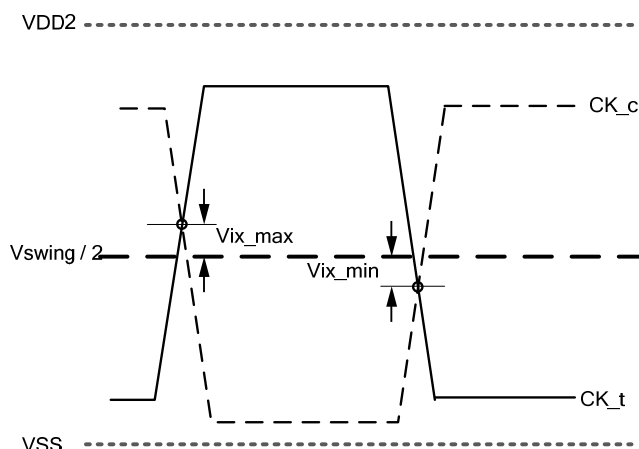


Figure 9 — CK input Crosspoint voltage (Vix)

Table 6 — CK input voltage crosspoint (Vix) ratio

Parameter	Symbol	Min	Max	Units	Notes
Clock Differential input crosspoint voltage ratio	Vix_CK_ratio	-	25	%	1,2
NOTE 1 The Vix voltage is referenced to $V_{swing}/2(avg) = 0.5(V_{CK_t} + V_{CK_c})$ where the average is over TBD ² UI.					
NOTE 2 The ratio of the Vix pk voltage divided by V_{diff_CK} : $Vix_CK_Ratio = 100 * (Vix_CK / V_{diff_CK})$ where $V_{diff_CK} \text{ pk-pk} = 2 * V_{CK_t} - V_{CK_c} $					

2.8 Internal Reference Voltage Ranges

LVSTL interface use internal generated Reference Voltage (Vref) for single ended signals. Vref Range should be min 15% of VDDQ to 62.9% of VDDQ. Internal Vref should be adjusted to suitable value.

At time of publication the formulating committee has not defined the value.

² At time of publication the formulating committee has not defined the value.

2.9 Overshoot and Undershoot

Table 7 — AC Overshoot/Undershoot Specification

Parameter			Units
Maximum peak amplitude allowed for overshoot area. (See Figure 10)	Max	0.3	V
Maximum peak amplitude allowed for undershoot area. (See Figure 10)	Max	0.3	V
Maximum area above VDD. (See Figure 10)	Max	0.1	V-ns
Maximum area below VSS. (See Figure 10)	Max	0.1	V-ns
NOTE 1 VDD2 stands for VDD for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. VDD stands for VDDQ for DQ, DMI, DQS_t and DQS_c.			
NOTE 2 VSS stands for VSS for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. VSS stands for VSSQ for DQ, DMI, DQS_t and DQS_c.			
NOTE 3 Maximum peak amplitude values are referenced from actual VDD and VSS values.			
NOTE 4 Maximum area values are referenced from maximum operating VDD and VSS values.			

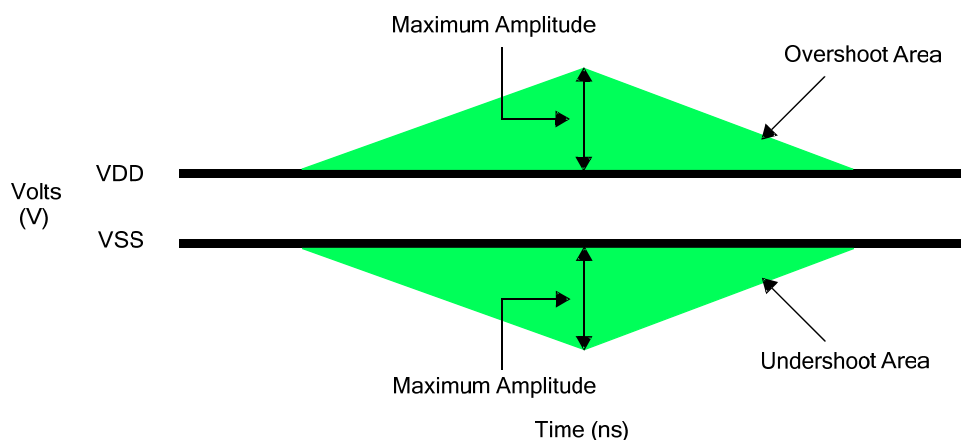


Figure 10 — Overshoot and Undershoot Definition



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